Board 2 Report

Zane McMorris*
Practical PCB Design and Manufacture
University of Colorado Boulder

March 2024

Contents

1 Project Overview **2**

2 Measurements and Results **4**
2.1 555 Timer Characteristics 4
2.2 PDN Switching Noise 4
2.3 Quiet Low and Quiet High Analysis 6

3 Extra Credit: Thevenin Equivalent Model **9**
3.1 RF Emissions 9

4 Conclusion **10**

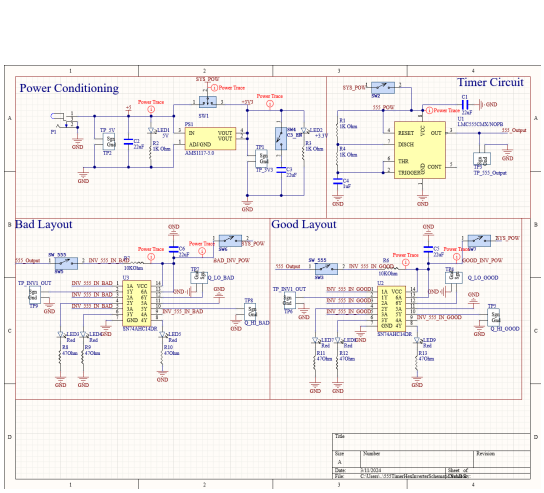
*ID: 109839099

1 Project Overview

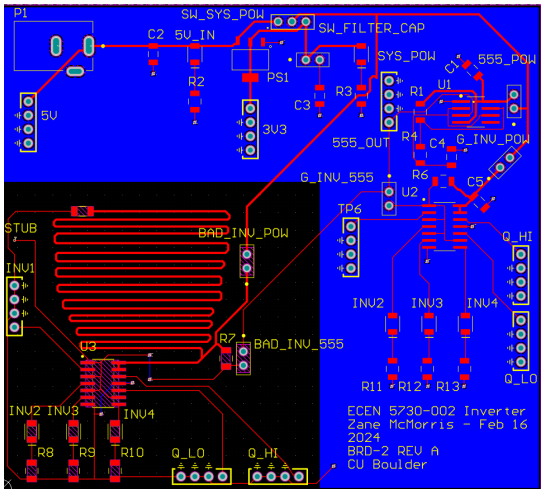
In this lab, I will validate that the second board I designed "works" according to the basic performance standards I have set and compare the differences between good layout techniques and bad. To work, the board must meet the following criteria. An important feature of this board is the intentionally poor design of half the board. The three key features that make it so abhorrent are the distance of the decoupling capacitor to the IC being powered, the lack of a ground plane, and the sharing of a return path. When not properly avoided, these three features can cause hard errors in the board's performance, and building these habits with the good side is important. But what's more important is knowing *why* it's bad and having something to compare the good layout to, which is why we have the poorly laid out portion of the board.

1. 5V is delivered to the board through the standard barrel-jack connector
2. 3.3V may be selected using a switch to choose either 5V or 3.3V system power.
3. The 555 timer delivers a duty cycle of 66% and a frequency of 500hz.
4. PDN noise is less than 10% of the target voltage
5. The hex inverters have system power delivered to them. Their first inverter output matches the logical NOT of the 555 signal.
6. All LEDs attached to the hex inverters are lit
7. All test points are connected and allow accurate measurement of the various signals
8. Signals from the "Bad" layout can be accurately and fairly compared to signals from the "good" layout

To accomplish these goals, I designed the board in Altium using the previous lab work on the hex inverter circuit as a reference. One of the new parts on this board was the low drop out (LDO), which converted 5V to 3.3V. Choosing between the two power networks was nice for testing the effects of different driving voltages on the components. I used the following schematic and made a 3.9" x 3.9" board for my layout to be conservative for my first real board. I ended up with lots of space, but it was a good learning opportunity to find what interconnect density I was comfortable with. One extra feature I added to my board that wasn't required and that I didn't expect good results from was my stub antenna. I am taking High-Speed Digital Design this semester, so we covered stubs briefly when I was building this board. I wanted to see the effects of the stub from the 500hz signal from the 555 timer. I will cover these results in the extra credit portion of the lab.

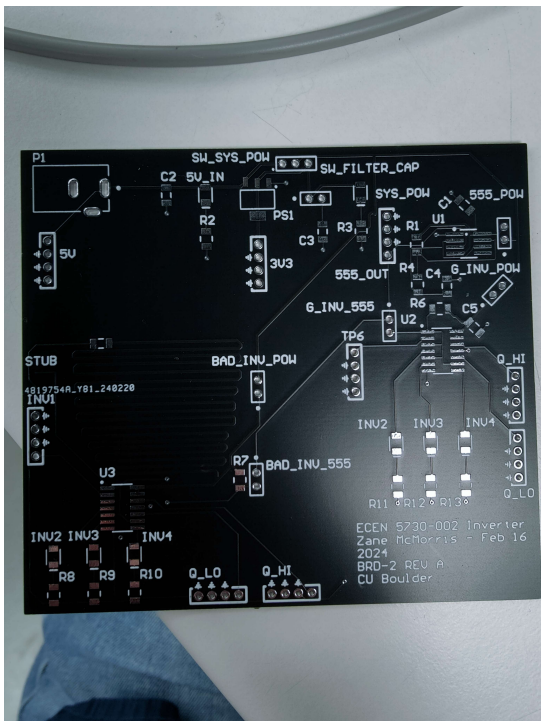


(a) Altium Schematic

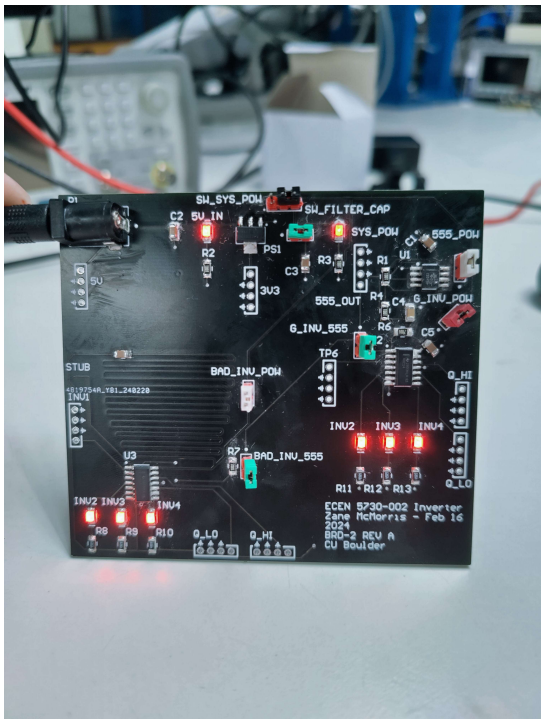


(b) Altium PCB Layout

Figure 1: PCB Schematic and layout



(a) Bare Board



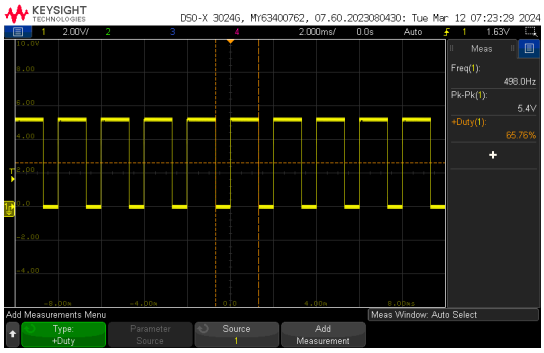
(b) Assembled board

Figure 2: Bare and assembled PCBs

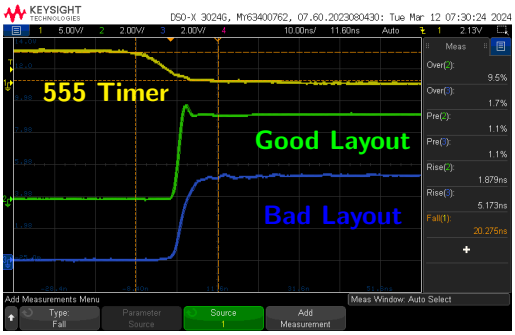
2 Measurements and Results

2.1 555 Timer Characteristics

After powering on the board and verifying that all my LEDs were lit up with no difference in brightness, I measured the duty cycle, frequency, rise and fall times, pre-shoot and overshoot, and any ripples or artifacts in the signal. I confirmed that the 555 timer precisely matched my expectation of 500hz and 66% duty cycle. The board performed better than my solderless breadboard (SBB) version of the circuit by being closer to our desired parameters.



(a) Duty Cycle and Frequency

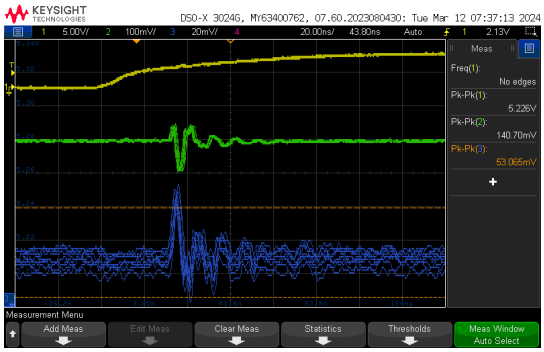


(b) Fall time & Rise Time of inverters

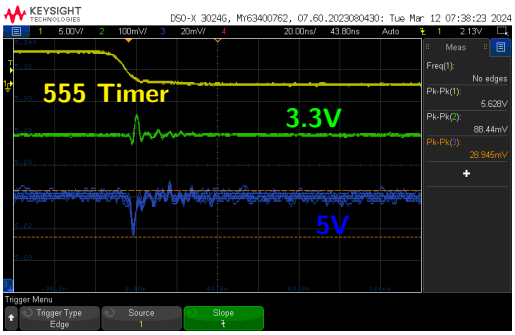
Figure 3: Characteristics of the 555 timer

2.2 PDN Switching Noise

After concluding that my 555 timer and inverter circuits were operating as expected, I measured the switching noise on the PDN for the 5V and 3.3V system inputs. The LDO that creates the 3.3V net is known to have some noise on its output, so a small filter capacitor is suggested to filter out the higher frequency noise, which I toggled on and off during this experiment.

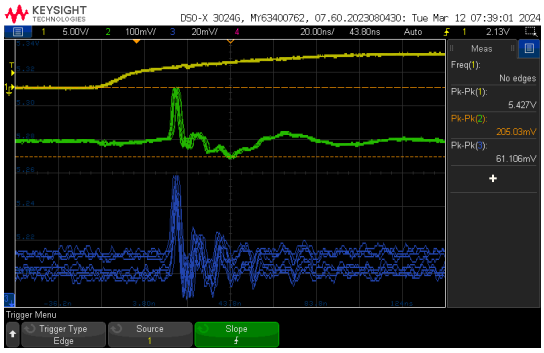


(a) Rising edge of clock signal

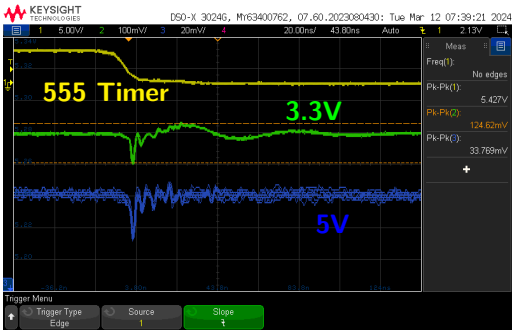


(b) Falling edge of clock signal

Figure 4: 3.3V & 5V PDN switching noise w/ LDO filter cap



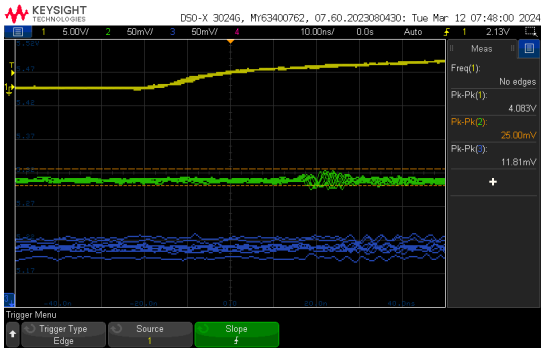
(a) Rising edge of clock signal



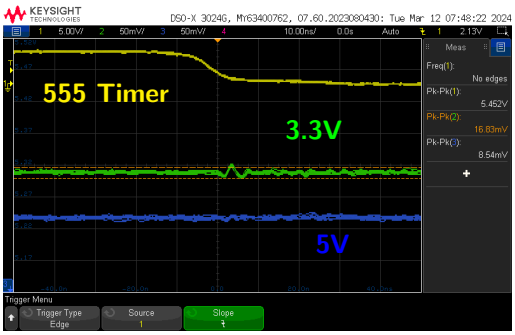
(b) Falling edge of clock signal

Figure 5: 3.3V & 5V PDN switching noise w/o LDO filter cap

Comparing the two figures, we can see that noise is abundant in the case of no filter cap. I can see multiple bouncing frequencies in the 3.3V rail, with at least two being the strongest. I can see one with roughly 40ns and another with about 10ns. I thought that these results were what I was looking for, but I thought about the effects of the bad layout on these measurements. I wanted to see what it would've been like with only the good layout, and the results were surprising.

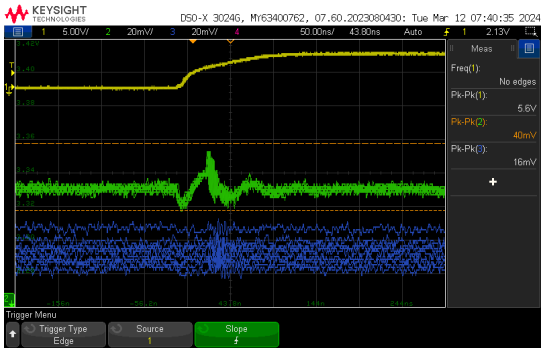


(a) Rising edge of clock signal

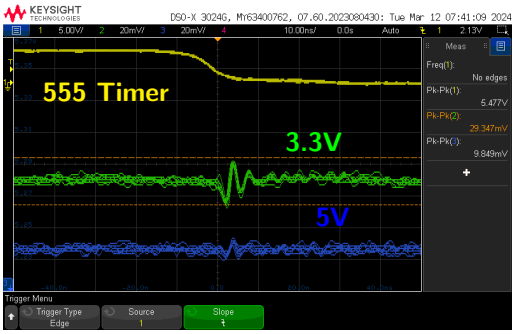


(b) Falling edge of clock signal

Figure 6: 3.3V & 5V PDN switching noise w/ LDO filter cap and no bad layout



(a) Rising edge of clock signal



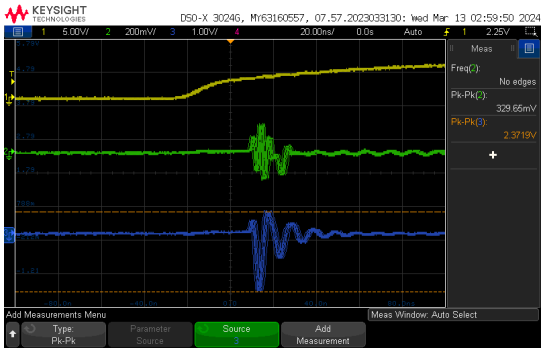
(b) Falling edge of clock signal

Figure 7: 3.3V & 5V PDN switching noise w/o LDO filter cap and no bad layout

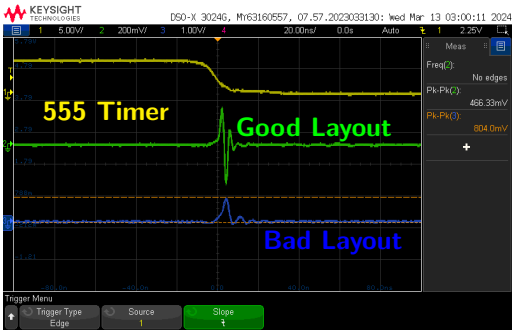
Now, the effects of the bad layout will become more obvious once we get rid of that filter cap for the LDO. I am not 100% sure of the effects and artifacts the LDO may cause, so I can only make educated guesses as to why the noise is taking the form that it is. Comparing the two sets also shows what positive effect the filter is having on the 3.3V signal. The worst case is with the bad layout attached and no filter cap. Here, we can see transients lasting about 120ns for both the rising and falling clock signal cases with a peak-to-peak (P2P) voltage of 205mV on the rising edge and 124mV on the falling edge. The 5V noise on the rising edge was greater than the falling edge by a factor of two, but the key features didn't differ much between the two cases. The second worst case was when the bad layout was disconnected and there was no filter cap on the LDO. Here, we can see the noise of the LDO the best because only the load from the good layout is present. This noise on the 3.3V rail lasted about 80ns on the rising edge and about 100ns on the falling edge. The P2P voltage for the 3.3V rail was 40mV on the rising edge and 30mV on the falling edge. This significant lowering in P2P voltage is likely due to removing the long inductive traces on the bad layout, which causes voltage spikes on the clock edges. The 5V noise in the two cases differs between the rising and falling edges, with the falling edge being much more coherent over time.

2.3 Quiet Low and Quiet High Analysis

To measure the quiet high and low line noise, I used both the 5V and 3.3V system power and measured the P2P voltage on both the rising and falling edges of the clock signal. The measurements can be seen in the figures below.

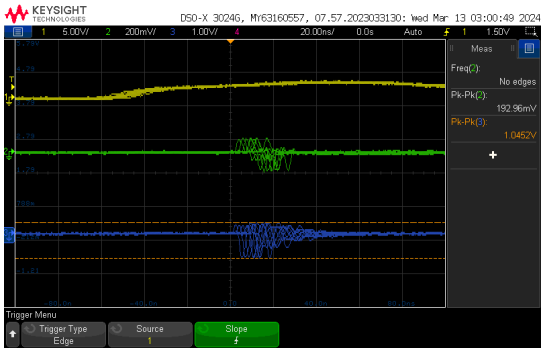


(a) Rising Edge

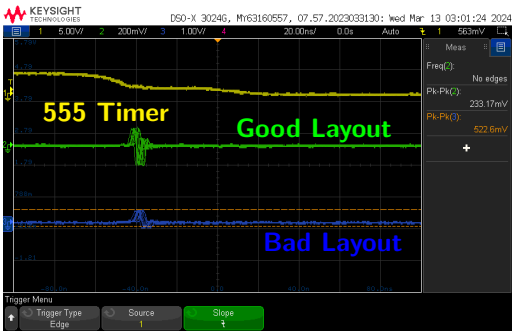


(b) Falling Edge

Figure 8: 5V Quiet High Noise Scope Pictures

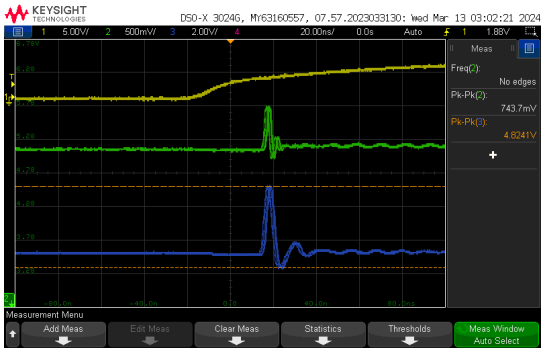


(a) Rising Edge

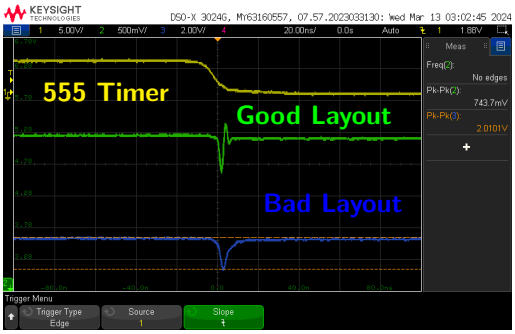


(b) Falling Edge

Figure 9: 3.3V Quiet High Noise Scope Pictures

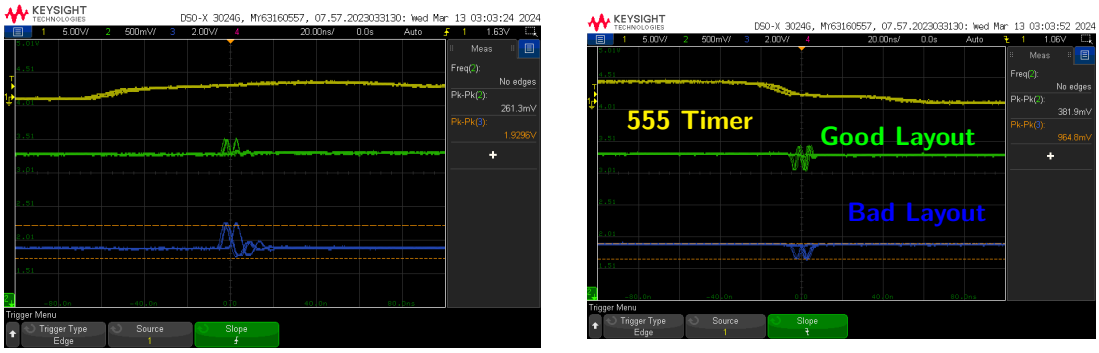


(a) Rising Edge



(b) Falling Edge

Figure 10: 5V Quiet Low Noise Scope Pictures



(a) Rising Edge

(b) Falling Edge

Figure 11: 3.3V Quiet Low Noise Scope Pictures

The noise on the bad layout portion of the board had a P2P amplitude that was generally twice that of the good layout and usually lasted longer. These large spikes in voltage are due to the extremely long inductive traces that the bad layout uses to connect everything, especially the return path. The return path for the bad side is shared for all the signals and is filled with conflicting signals. The results of this experiment further cement how important keeping trace lengths low and having a continuous ground plane is.

3 Extra Credit: Thevenin Equivalent Model

One extra credit opportunity was determining the Thevenin equivalent circuit for the single inverter as a source. To accomplish this, I wrote the simple circuit pictured to the right and figured out what points to probe and how to hook it up properly. First, I measured the open circuit voltage and found it to be 5.24V. I then measured the voltage at the positive end of the LED and found it to be 3.95V, and I found the negative end to be 1.81V. Finally, I measured the 49Ωresistor with a digital multimeter (DMM) and found the resistance to be 49.96Ω, nearly exactly 50Ω. Using this resistance and voltage drop, the current must be 36.2mA. Given that the positive side of the LED, the source voltage, was 3.95V, the Thevenin resistance is 35.6Ω.

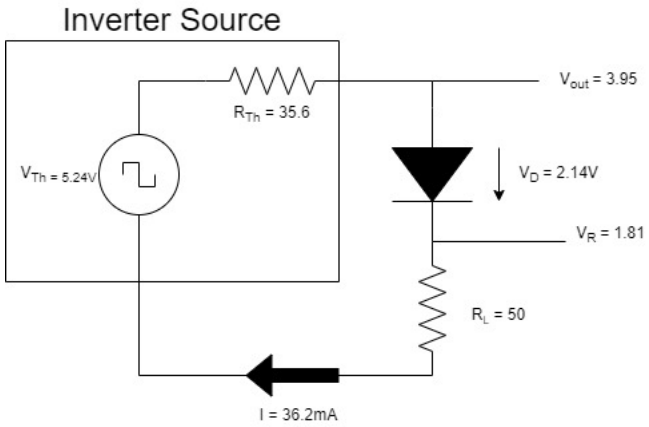


Figure 12: Thevenin Equivalent Circuit Model

3.1 RF Emissions

The stub I added on the PCB was very small and is pictured in figure 13. As a part of the high-speed class, I simulated a roughly equivalent circuit and found that reflections should be minimal, up to 300MHz or so, and nowhere near the 500hz clock signal.

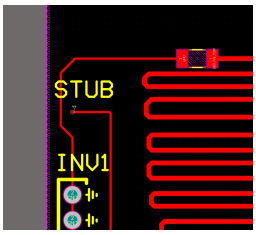
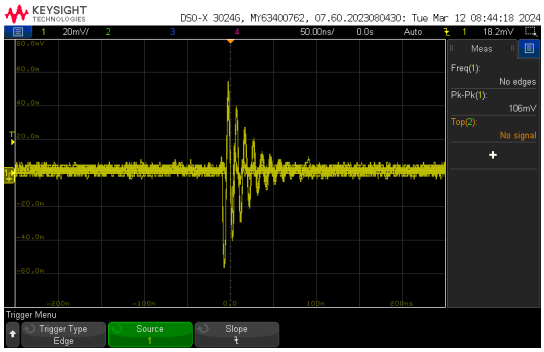


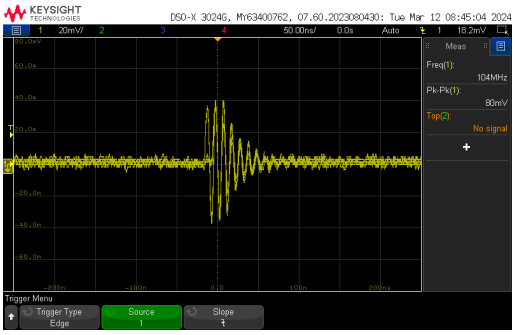
Figure 13: Stub location on PCB

Using a 10x scope probe clipped to itself, I had a small, highly sensitive inductive loop hooked up to the probe. I sniffed around the stub and found a small signal corresponding to the clock edge! I kept sniffing

around the board to see if it was a fluke, but I found another, slightly weaker signal near the quiet high test point at the bottom of the board.



(a) Signal from stub



(b) Signal from quiet high

Figure 14: Results of crude RF test

The P2P voltage off the stub was about 100mV, and the test point was 80mV. The two waveforms were nearly identical, but the test point was less defined, and there was a bit of noise.

4 Conclusion

Overall, I am very happy with the resulting board. My bad layout was sufficiently poor to yield good results, and my good layout was good enough to have minimal noise. I learned some good techniques for placing sections modularly and keeping the footprint small. Routing a couple of small ICs with tight legs gives us brief experience before we hit the Arduino board, where we have to route a much more complicated IC. I'm also glad I could see something from my stub antenna because that's something I did just for fun.

Some things I do better in future boards will be to route traces more cleanly and group them together when I have signals going in the same direction for aesthetics and better organization. I'll pay more attention to the placement of the decoupling capacitor.